

# GA-78LMT-S2

**Revision : 1.21**

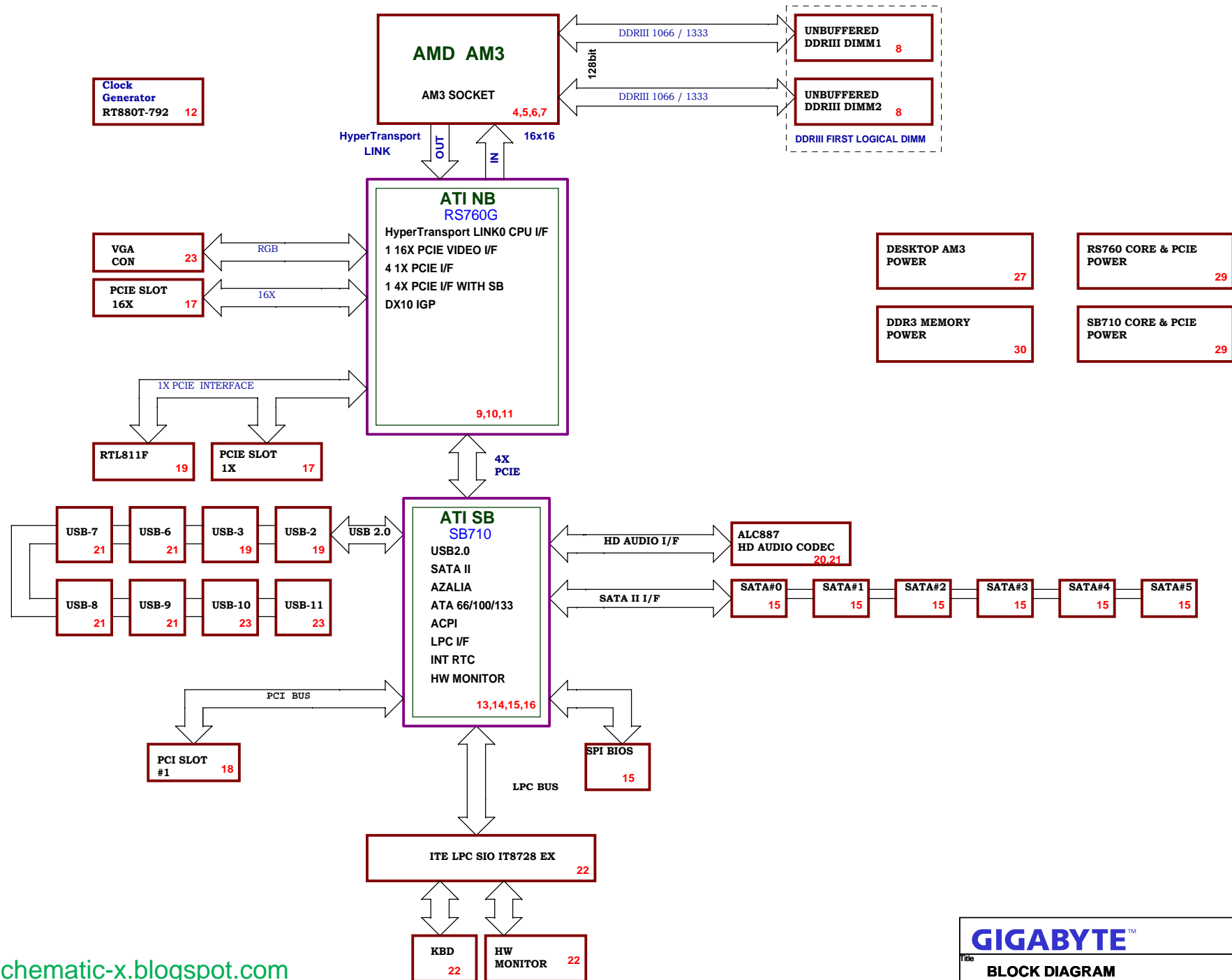
PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A0, B0
09	RS780 HT-LINK I/F
10	RS780 SYSTEM I/F,STRAP,DVI
11	RS780 POWER & GND
12	IDT 9LPRS485C
13	ATI SB710 PCIE/PCI/CPU/LPC/CLK
14	ATI SB710 ACPI/USB/GPIO/AUDIO
15	ATI SB710 SATA/IDE/HWM/SPI
16	ATI SB710 POWER & GND
17	PCI EXPRESS x16 ,x1
18	PCI SLOT
19	LAN AR8151/8152
20	ALC887-VD2
21	RGB, COM, F_USB ,USB
22	IT8728DX,Dual-BIOS FAN/HWMO
23	ATX, FRONT PANEL
24	VCORE(RT8868+RT9612)
25	POWER SEQUENCE,EUP

[illegible]

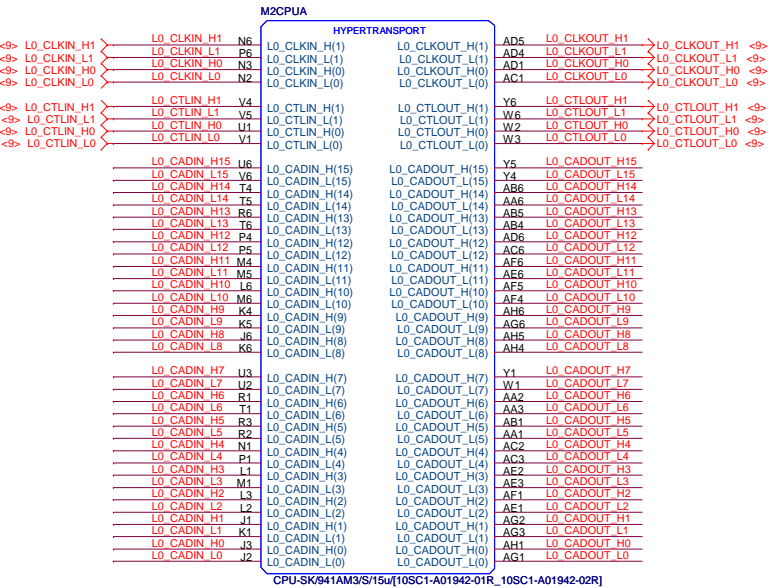
<b>GIGABYTE™</b>			
Title			
<b>COVER SHEET</b>			
Size	Document Number	Rev	
Custom	<b>GA-78LMT-S2</b>	<b>1.21</b>	
Date:	Tuesday, April 23, 2013	Sheet	1 of 27



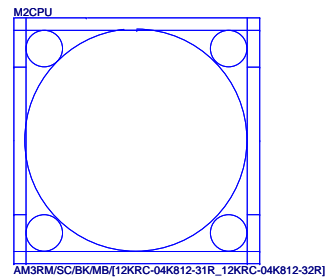
# RS780L CUSTOMER DESKTOP DESIGN

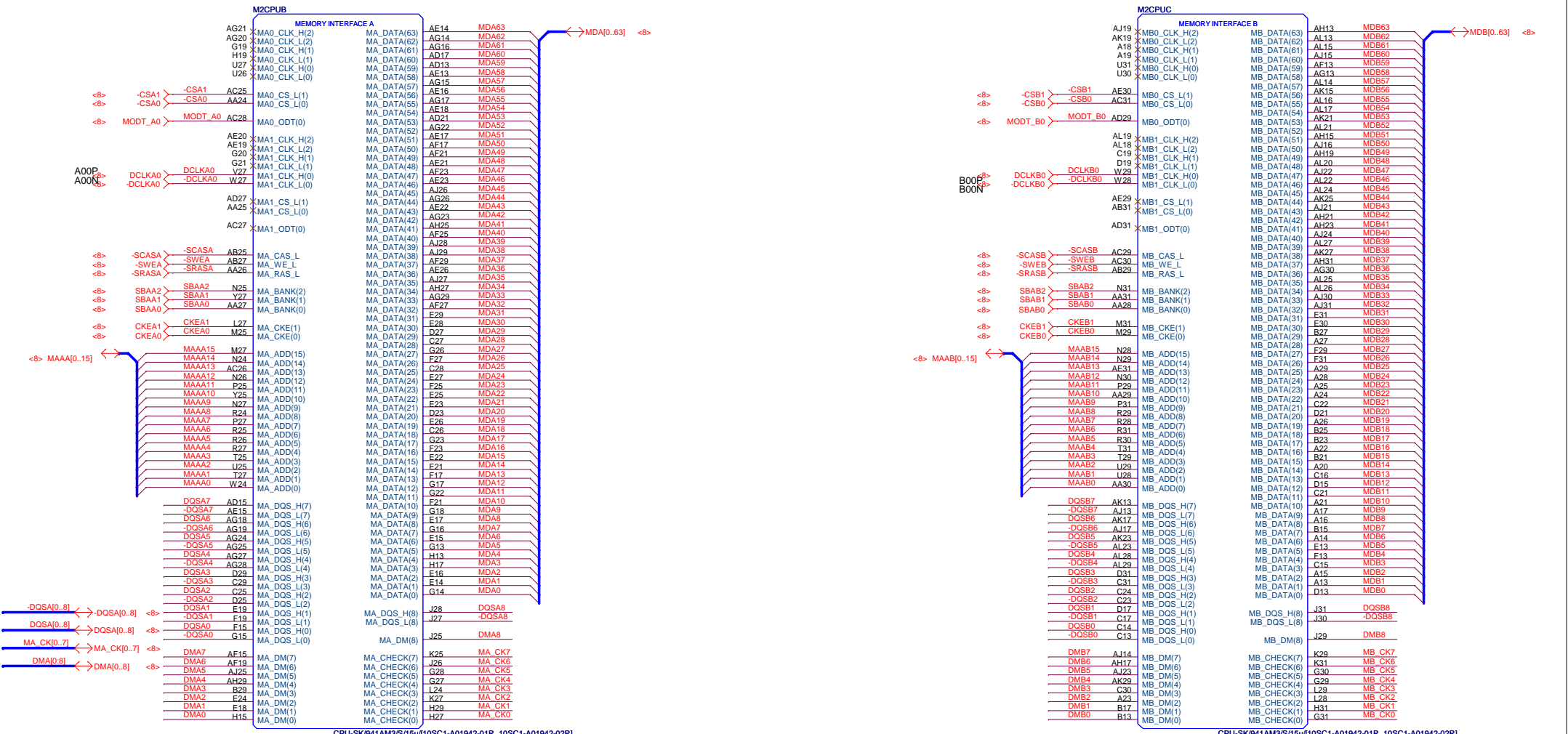


L0\_CADIN\_L[0..15] <9>  
L0\_CADIN\_H[0..15] <9>  
  
L0\_CADOUT\_L[0..15] <9>  
L0\_CADOUT\_H[0..15] <9>



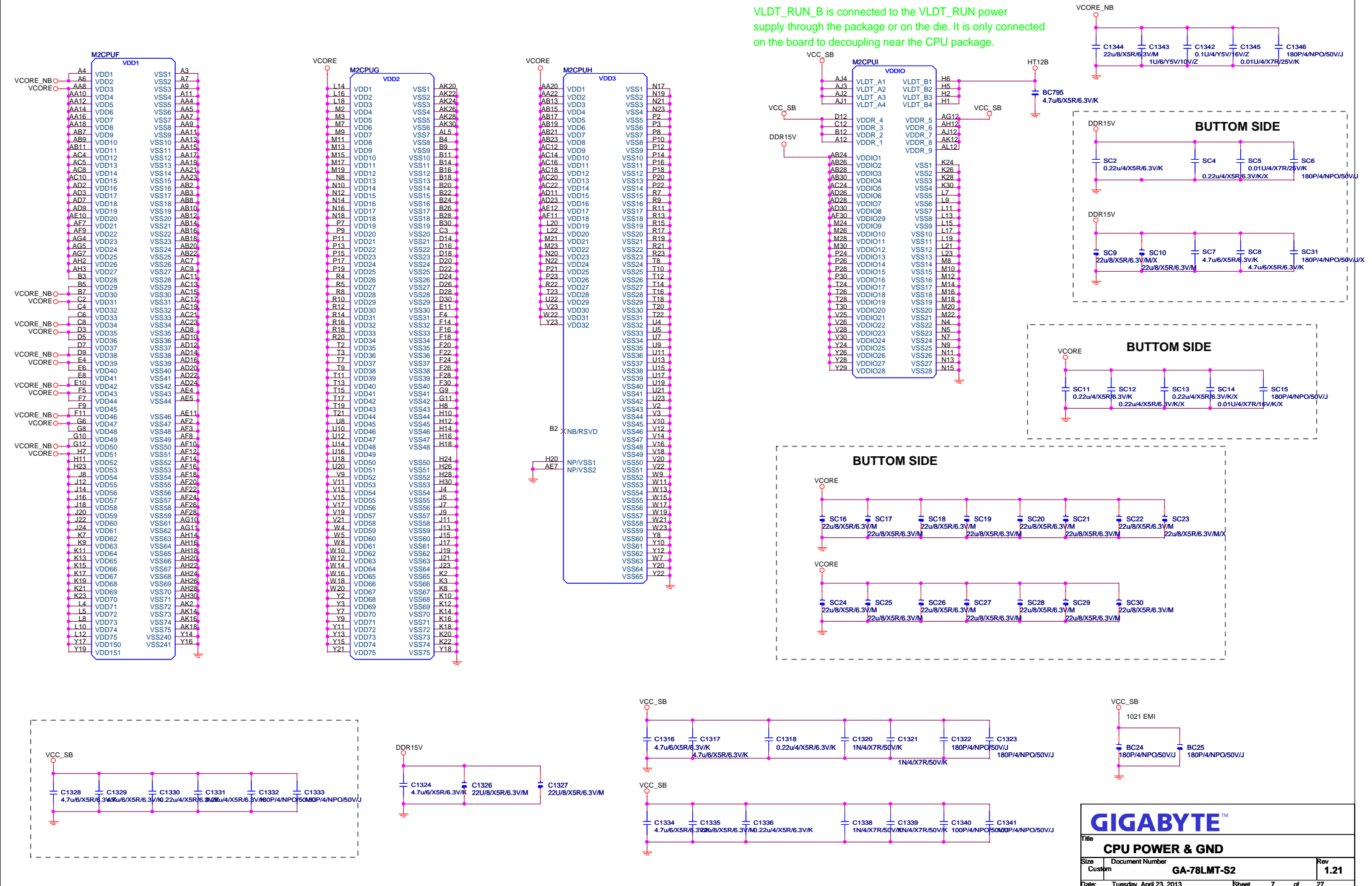
CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR18V  
CPU\_VTT\_SUS = DDRVTT  
  
VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B







VLDT\_RUN\_B is connected to the VLDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.







L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] <4>  
L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] <4>  
L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] <4>  
L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] <4>

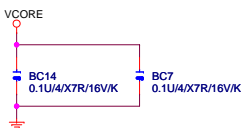
U3A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

<4> L0\_CLKOUT\_H0 > L0\_CLKOUT\_H0 T22 HT\_RXCLK0P  
<4> L0\_CLKOUT\_L0 > L0\_CLKOUT\_L0 T23 HT\_RXCLK0N  
<4> L0\_CLKOUT\_H1 > L0\_CLKOUT\_H1 AB23 HT\_RXCLK1P  
<4> L0\_CLKOUT\_L1 > L0\_CLKOUT\_L1 AA22 HT\_RXCLK1N  
L0\_CTOUT\_H0 > L0\_CTOUT\_H0 M22 HT\_RXCTL0P  
L0\_CTOUT\_L0 > L0\_CTOUT\_L0 M23 HT\_RXCTL0N  
L0\_CTOUT\_H1 > L0\_CTOUT\_H1 R21 HT\_RXCTL1P  
L0\_CTOUT\_L1 > L0\_CTOUT\_L1 R20 HT\_RXCTL1N  
R267 301/4/1 HT\_RXCALP C23 HT\_RXCALP  
HT\_RXCALN A24 HT\_RXCALN

RS780L/FCBGA528/A13/[10HB1-06760G-20R]



HT\_TXCAD0P D24 L0\_CADIN\_H0  
HT\_TXCAD0N D25 L0\_CADIN\_L0  
HT\_TXCAD1P E24 L0\_CADIN\_H1  
HT\_TXCAD1N E25 L0\_CADIN\_L1  
HT\_TXCAD2P F24 L0\_CADIN\_H2  
HT\_TXCAD2N F25 L0\_CADIN\_L2  
HT\_TXCAD3P F23 L0\_CADIN\_H3  
HT\_TXCAD3N F22 L0\_CADIN\_L3  
HT\_TXCAD4P H22 L0\_CADIN\_H4  
HT\_TXCAD4N H23 L0\_CADIN\_L4  
HT\_TXCAD5P J25 L0\_CADIN\_H5  
HT\_TXCAD5N J24 L0\_CADIN\_L5  
HT\_TXCAD6P K24 L0\_CADIN\_H6  
HT\_TXCAD6N K25 L0\_CADIN\_L6  
HT\_TXCAD7P K23 L0\_CADIN\_H7  
HT\_TXCAD7N K22 L0\_CADIN\_L7  
HT\_TXCAD8P F21 L0\_CADIN\_H8  
HT\_TXCAD8N G21 L0\_CADIN\_L8  
HT\_TXCAD9P G20 L0\_CADIN\_H9  
HT\_TXCAD9N H21 L0\_CADIN\_L9  
HT\_TXCAD10P J21 L0\_CADIN\_H10  
HT\_TXCAD10N J18 L0\_CADIN\_H11  
HT\_TXCAD11P K17 L0\_CADIN\_L10  
HT\_TXCAD11N K19 L0\_CADIN\_L11  
HT\_TXCAD12P L19 L0\_CADIN\_H12  
HT\_TXCAD12N L19 L0\_CADIN\_L12  
HT\_TXCAD13P M19 L0\_CADIN\_H13  
HT\_TXCAD13N L18 L0\_CADIN\_L13  
HT\_TXCAD14P M21 L0\_CADIN\_H14  
HT\_TXCAD14N P21 L0\_CADIN\_L14  
HT\_TXCAD15P P18 L0\_CADIN\_H15  
HT\_TXCAD15N M18 L0\_CADIN\_L15  
HT\_TXCLK0P H24 L0\_CLKIN\_H0 > L0\_CLKIN\_H0 <4>  
HT\_TXCLK0N H25 L0\_CLKIN\_L0 > L0\_CLKIN\_L0 <4>  
HT\_TXCLK1P L21 L0\_CLKIN\_H1 > L0\_CLKIN\_H1 <4>  
HT\_TXCLK1N L20 L0\_CLKIN\_L1 > L0\_CLKIN\_L1 <4>  
HT\_TXCTL0P M24 L0\_CTLIN\_H0 > L0\_CTLIN\_H0 <4>  
HT\_TXCTL0N M25 L0\_CTLIN\_L0 > L0\_CTLIN\_L0 <4>  
HT\_TXCTL1P P19 L0\_CTLIN\_H1 > L0\_CTLIN\_H1 <4>  
HT\_TXCTL1N R18 L0\_CTLIN\_L1 > L0\_CTLIN\_L1 <4>  
B24 HT\_TXCALP R268 301/4/1  
B25 HT\_TXCALN

<17> PCIE2\_IP >  
<17> PCIE2\_IN >  
<19> ML\_IP >  
<19> ML\_IN >

<13> A\_RX0P > A\_RX0P AA8  
<13> A\_RX0N > A\_RX0N Y8  
<13> A\_RX1P > A\_RX1P AA7  
<13> A\_RX1N > A\_RX1N Y7  
<13> A\_RX2P > A\_RX2P AA6  
<13> A\_RX2N > A\_RX2N W5  
<13> A\_RX3P > A\_RX3P W5  
<13> A\_RX3N > A\_RX3N Y5

EXP\_A\_RXP[0..15] >> EXP\_A\_RXP[0..15] <17>  
EXP\_A\_RXN[0..15] >> EXP\_A\_RXN[0..15] <17>  
EXP\_A\_TXP[0..15] >> EXP\_A\_TXP[0..15] <17>  
EXP\_A\_TXN[0..15] >> EXP\_A\_TXN[0..15] <17>

U3B  
EXP\_A\_RXP0 D4 GFX\_RX0P  
EXP\_A\_RXN0 C4 GFX\_RX0N  
EXP\_A\_RXP1 A3 GFX\_RX1P  
EXP\_A\_RXN1 B3 GFX\_RX1N  
EXP\_A\_RXP2 C2 GFX\_RX2P  
EXP\_A\_RXN2 C1 GFX\_RX2N  
EXP\_A\_RXP3 C1 GFX\_RX2N  
EXP\_A\_RXN3 F5 GFX\_RX3P  
EXP\_A\_RXP4 G5 GFX\_RX3N  
EXP\_A\_RXN4 G6 GFX\_RX4P  
EXP\_A\_RXP5 H5 GFX\_RX4N  
EXP\_A\_RXN5 H6 GFX\_RX5P  
EXP\_A\_RXP6 J6 GFX\_RX5N  
EXP\_A\_RXN6 J5 GFX\_RX6P  
EXP\_A\_RXP7 J7 GFX\_RX7P  
EXP\_A\_RXN7 J8 GFX\_RX7N  
EXP\_A\_RXP8 I5 GFX\_RX8P  
EXP\_A\_RXN8 I6 GFX\_RX8N  
EXP\_A\_RXP9 M8 GFX\_RX9P  
EXP\_A\_RXN9 L8 GFX\_RX9N  
EXP\_A\_RXP10 P7 GFX\_RX10P  
EXP\_A\_RXN10 M7 GFX\_RX10N  
EXP\_A\_RXP11 P5 GFX\_RX11P  
EXP\_A\_RXN11 M5 GFX\_RX11N  
EXP\_A\_RXP12 R8 GFX\_RX12P  
EXP\_A\_RXN12 P8 GFX\_RX12N  
EXP\_A\_RXP13 R6 GFX\_RX13P  
EXP\_A\_RXN13 R5 GFX\_RX13N  
EXP\_A\_RXP14 P4 GFX\_RX14P  
EXP\_A\_RXN14 P3 GFX\_RX14N  
EXP\_A\_RXP15 T4 GFX\_RX15P  
EXP\_A\_RXN15 T3 GFX\_RX15N  
GPP\_RX0P AC1  
GPP\_RX0N AC2  
GPP\_RX1P AB4  
GPP\_RX1N AB3  
GPP\_RX2P AA2  
GPP\_RX2N AA1  
GPP\_RX3P Y1  
GPP\_RX3N Y2  
GPP\_RX4P Y4  
GPP\_RX4N V1  
GPP\_TX0P AC1  
GPP\_TX0N AC2  
GPP\_TX1P AB4  
GPP\_TX1N AB3  
GPP\_TX2P AA2  
GPP\_TX2N AA1  
GPP\_TX3P Y1  
GPP\_TX3N Y2  
GPP\_TX4P Y4  
GPP\_TX4N V1  
GPP\_TX5P V2  
GPP\_TX5N V2  
SB\_RX0P AD7  
SB\_RX0N AE7  
SB\_RX1P AE6  
SB\_RX1N AD6  
SB\_RX2P AD6  
SB\_RX2N AD5  
SB\_RX3P AD5  
SB\_RX3N AE5  
PCE\_CALRP(PCE\_BCALRP) AC8  
PCE\_CALRN(PCE\_BCALRN) AB8  
R210 1.27K/4/1  
R212 2K/4/1  
NB\_VCC

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

PLACE CAP CLOSE TO CONNECTOR

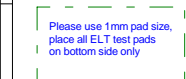
<17> PCIE2\_OP >  
<17> PCIE2\_ON >  
<19> ML\_OP >  
<19> ML\_ON >

<13> A\_TX0P > A\_TX0P C138  
<13> A\_TX0N > A\_TX0N C139  
<13> A\_TX1P > A\_TX1P C140  
<13> A\_TX1N > A\_TX1N C141  
<13> A\_TX2P > A\_TX2P C142  
<13> A\_TX2N > A\_TX2N C143  
<13> A\_TX3P > A\_TX3P C144  
<13> A\_TX3N > A\_TX3N C145

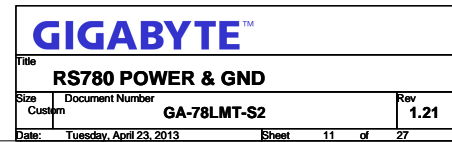
GIGABYTE™

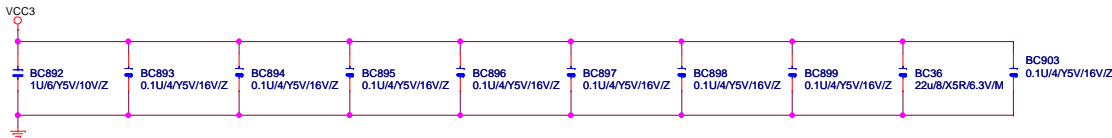
Title <b>RS780 HT-LINK I/F</b>		
Size Custom	Document Number <b>GA-78LMT-S2</b>	Rev <b>1.21</b>
Date: Tuesday, April 23, 2013 Sheet 9 of 27		



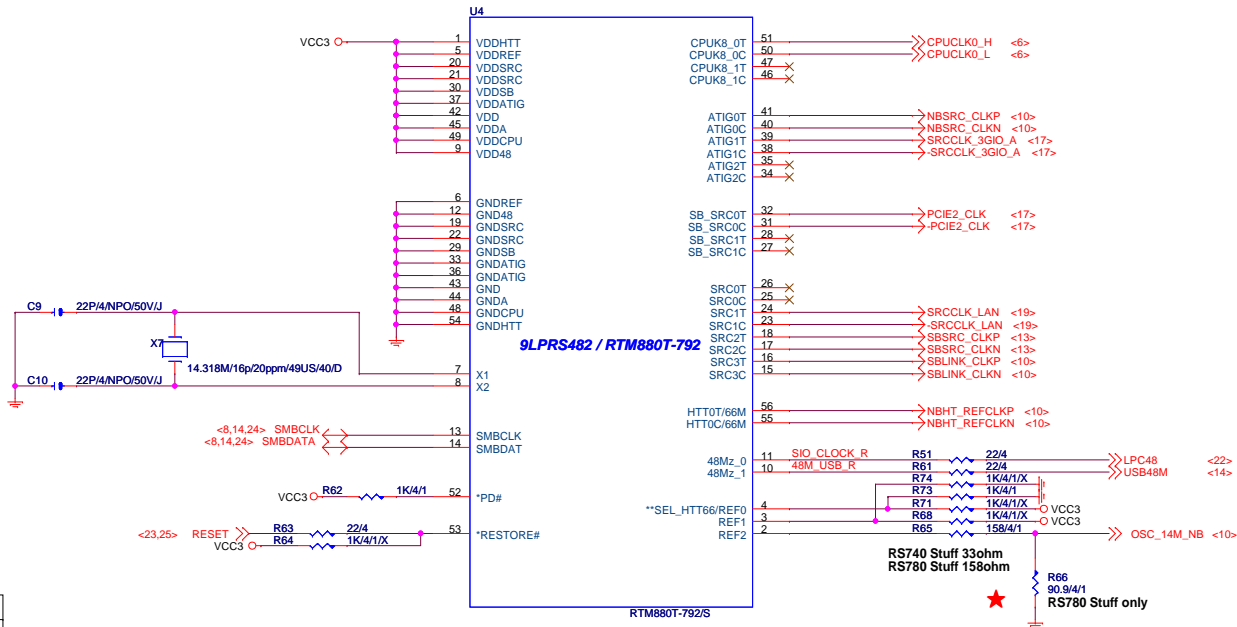


PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



watch dog --  
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

\* the GFX\_REFCLK input is required for all cases

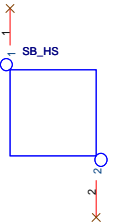
# GIGABYTE™

Title		RTM880T-792	
Size	Document Number	GA-78LMT-S2	
Custom		Rev 1.21	
Date:	Tuesday, April 23, 2013	Sheet	12 of 27

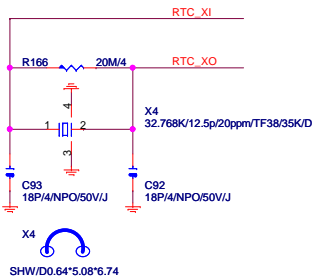


PLACE THESE PCIE AC COUPLING  
CAPS CLOSE TO U600

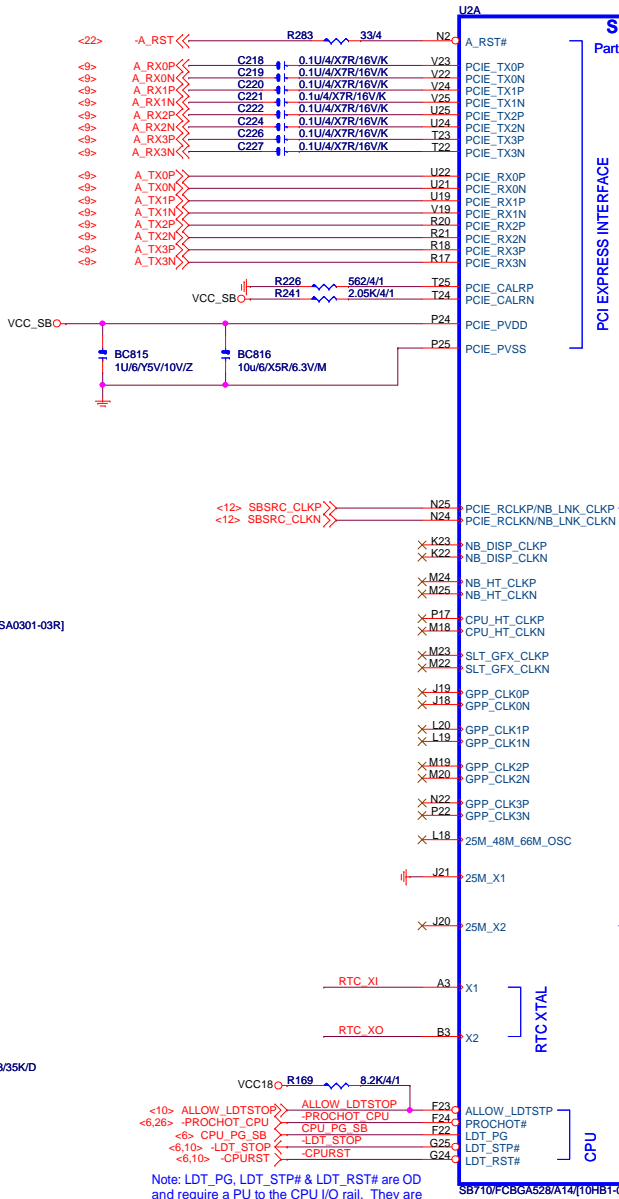
## S.B HEATSINK



SB\_HS[12SP2-SA0301-01R\_12SP2-SA0301-02R\_12SP2-SA0301-03R]

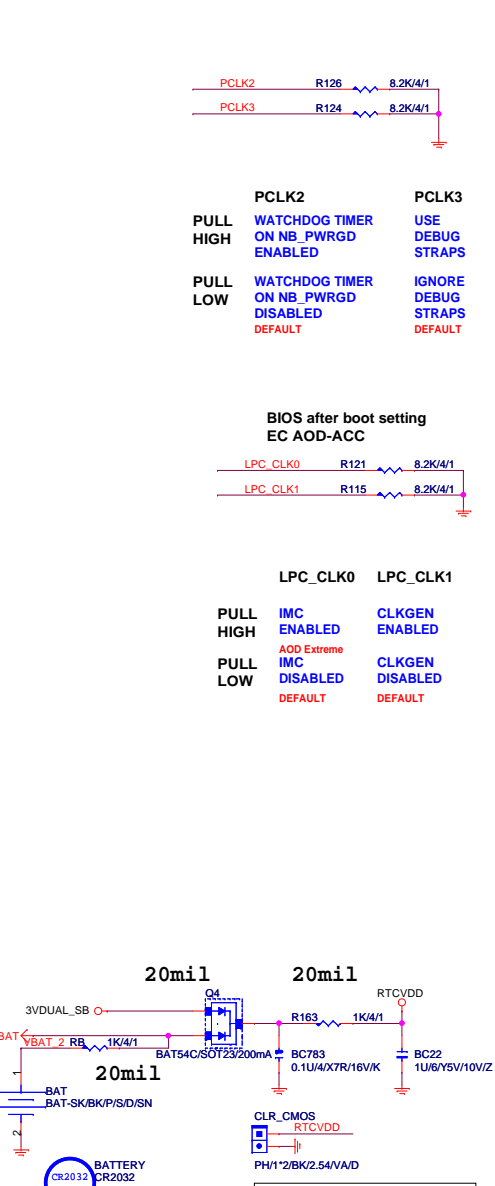
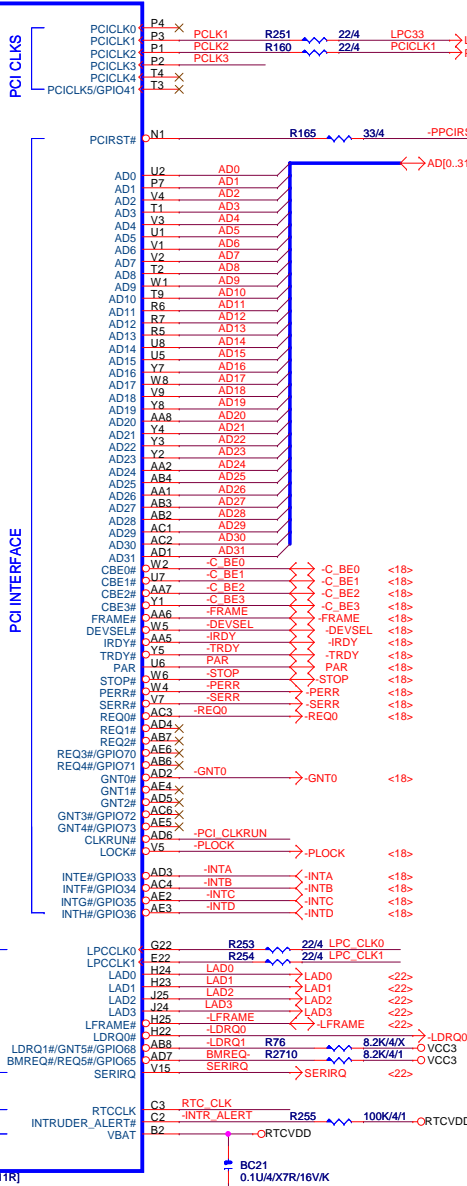


Note: LDT\_PG, LDT\_STP# & LDT\_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



## SB700

Part 1 of 5



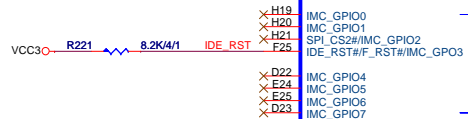
GIGABYTE™

ATI SB710 PCIE/PCI/CPU/LPC

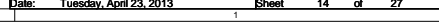
Size	Document Number	Rev
Custom	GA-78LMT-S2	1.21
Date:	Tuesday, April 23, 2013	Sheet 13 of 27



**PULL LOW**    **DISABLE PCI MEM BOOT**  
**DEFAULT**



L, L = FWH ROM





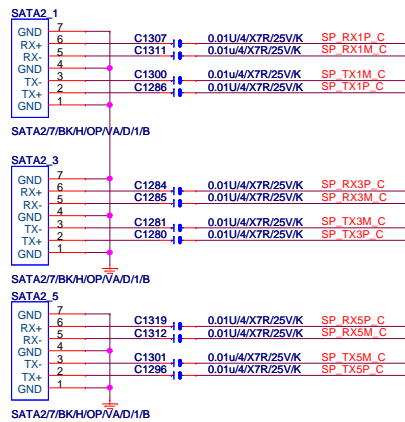
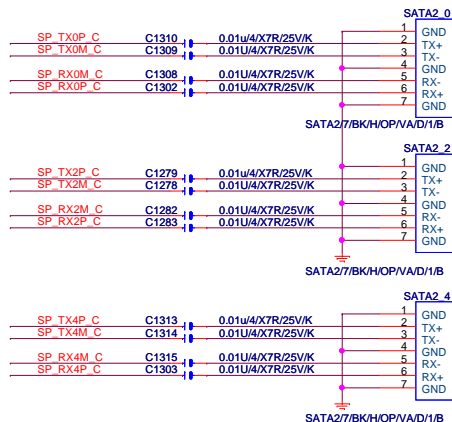
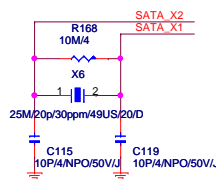
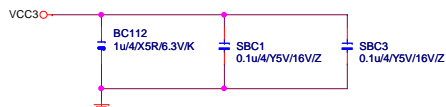
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600



PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

**NOTE:**

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



**SB700**  
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

IDE\_IORDY  
IDE\_IRQ  
IDE\_A0  
IDE\_A1  
IDE\_A2  
IDE\_DACK#  
IDE\_DRQ  
IDE\_IOR#  
IDE\_IOW#  
IDE\_CS1#  
IDE\_CS3#  
IDE\_D0/GPIO15  
IDE\_D1/GPIO16  
IDE\_D2/GPIO17  
IDE\_D3/GPIO18  
IDE\_D4/GPIO19  
IDE\_D5/GPIO20  
IDE\_D6/GPIO21  
IDE\_D7/GPIO22  
IDE\_D8/GPIO23  
IDE\_D9/GPIO24  
IDE\_D10/GPIO25  
IDE\_D11/GPIO26  
IDE\_D12/GPIO27  
IDE\_D13/GPIO28  
IDE\_D14/GPIO29  
IDE\_D15/GPIO30

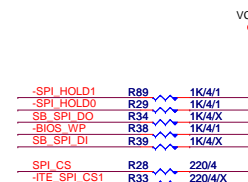
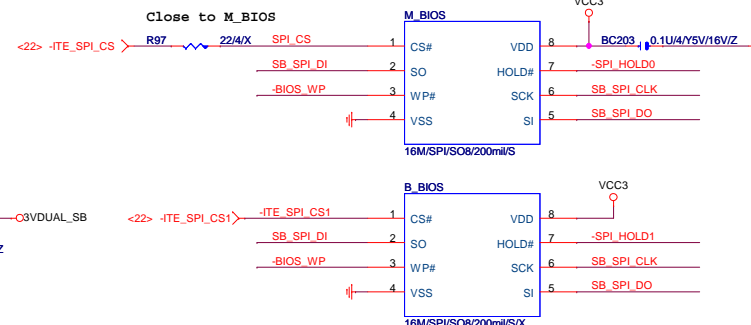
SPI\_DI/GPIO12  
SPI\_DO/GPIO11  
SPI\_CLK/GPIO47  
SPI\_HOLD#/GPIO31  
SPI\_CS1#/GPIO32  
LAN\_RST#/GPIO13  
ROM\_RST#/GPIO14  
FANOUT0/GPIO3  
FANOUT1/GPIO48  
FANOUT2/GPIO49  
FANIN0/GPIO50  
FANIN1/GPIO51  
FANIN2/GPIO52  
TEMP\_COMM  
TEMPIN0/GPIO61  
TEMPIN1/GPIO62  
TEMPIN2/GPIO63  
TEMPIN3/TALERT#/GPIO64  
VIN0/GPIO53  
VIN1/GPIO54  
VIN2/GPIO55  
VIN3/GPIO56  
VIN4/GPIO57  
VIN5/GPIO58  
VIN6/GPIO59  
VIN7/GPIO60

AVDD  
AVSS

AA24  
AA25  
Y22  
AB23  
Y23  
AB24  
AD25  
AC25  
AC24  
Y25  
Y24  
AD24  
AD23  
AE22  
AC22  
AD21  
AE20  
AB20  
AD19  
AE19  
AC20  
AD20  
AE21  
AB22  
AD22  
AE23  
AC23

PDD7 R189 8.2K/4/1

G6 SB SPI DI\_R R101 22/4 SB SPI DI  
D2 SB SPI DO\_R R102 22/4 SB SPI DO  
D1 SB SPI CLK\_R R92 22/4 SB SPI CLK  
F4 SB SPI CS R103 22/4/X SB SPI CS\_ITE <22>  
U15 R96 22/4 SPI\_CS



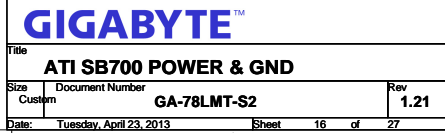
**GIGABYTE**™

ATI SB710 SATA/IDE/HWM/SPI

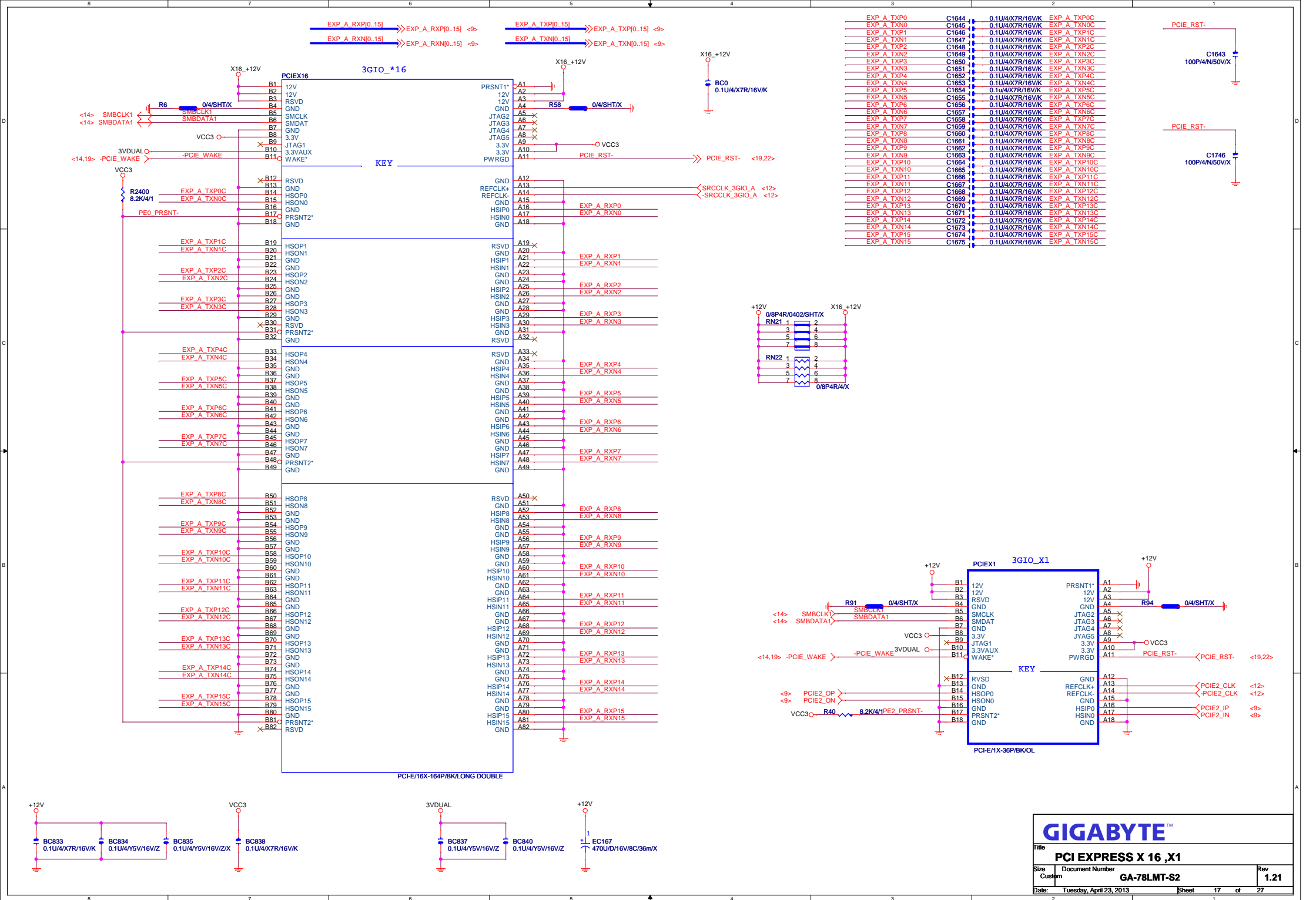
Size Custom Document Number GA-78LMT-S2 Rev 1.21

Date: Tuesday, April 23, 2013 Sheet 15 of 27

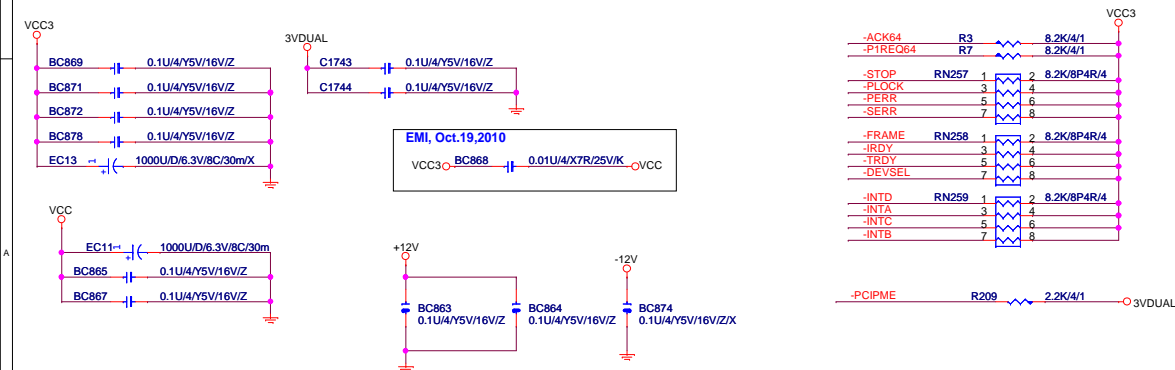
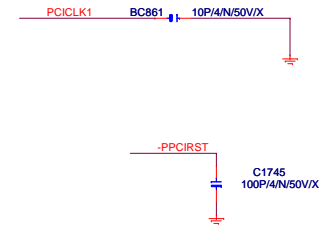
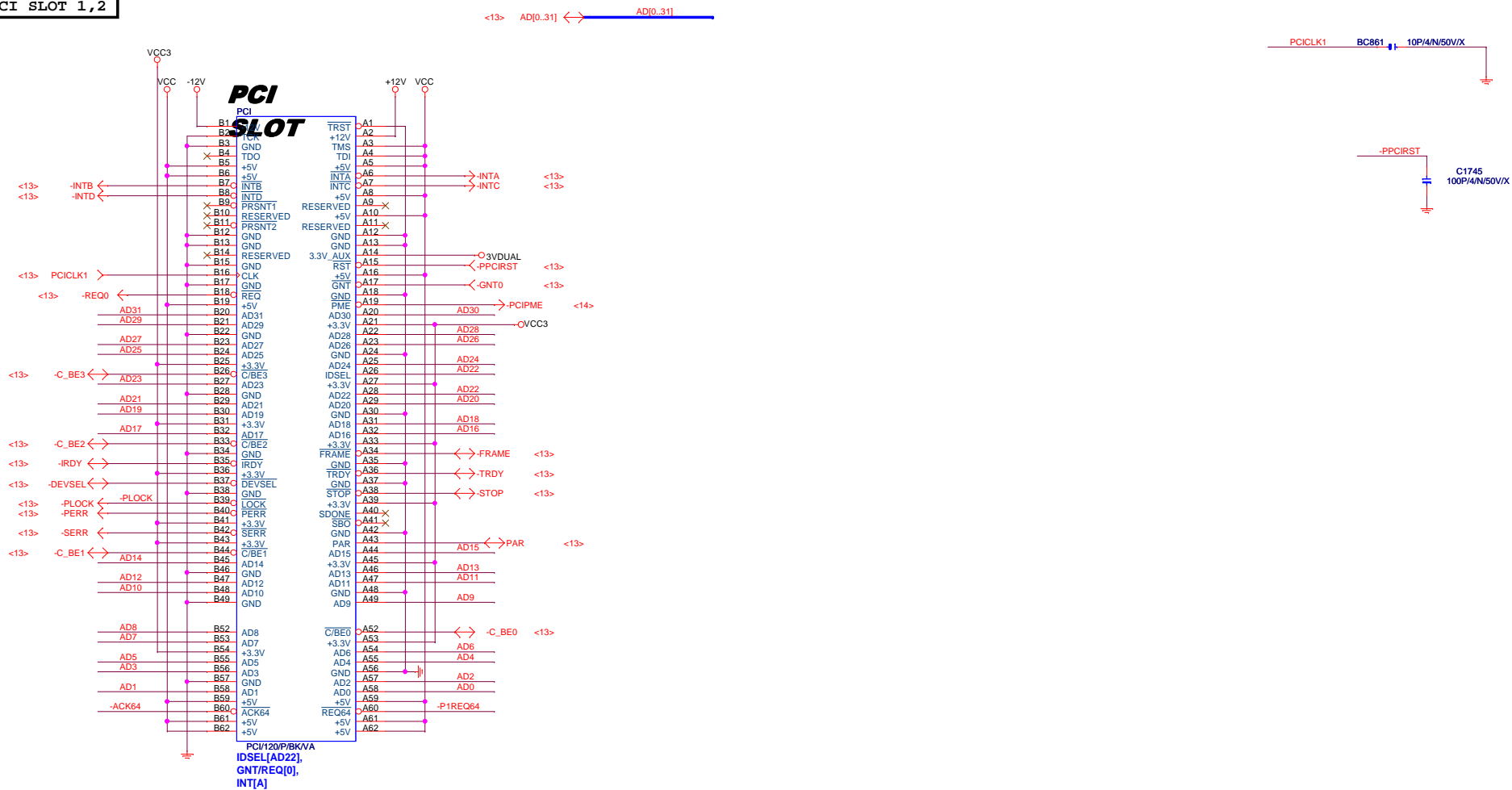






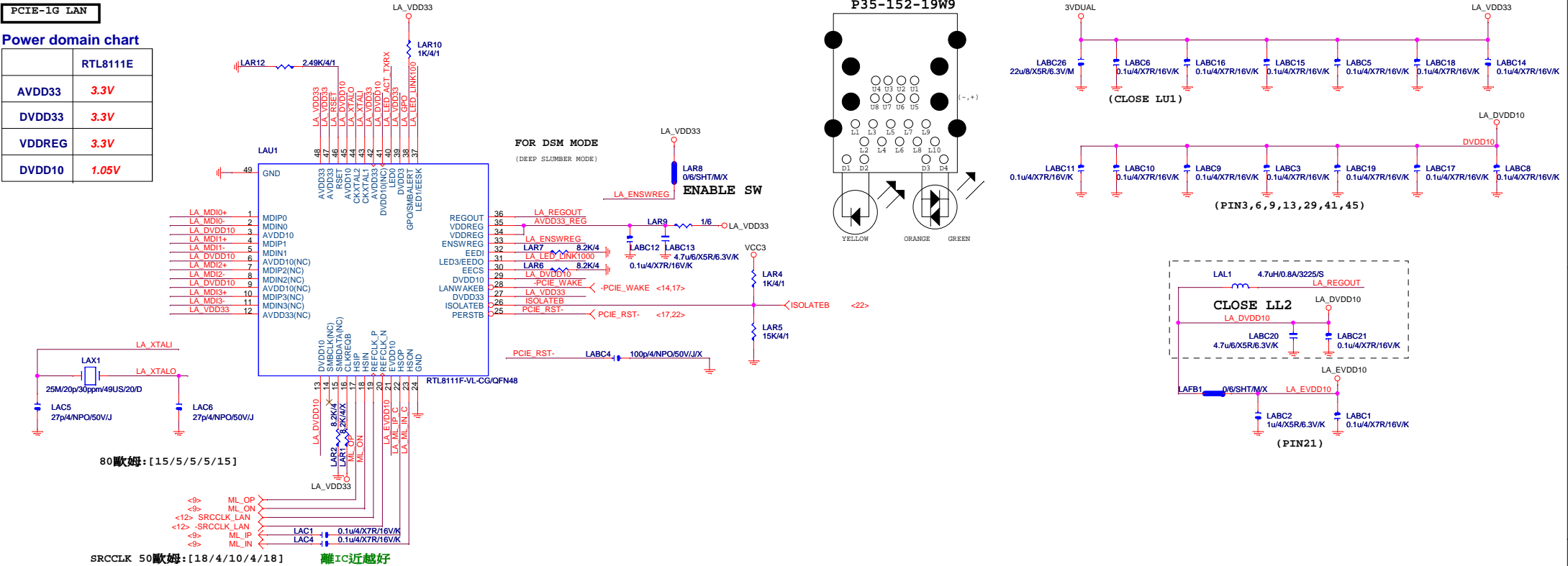


PCI SLOT 1,2
--------------

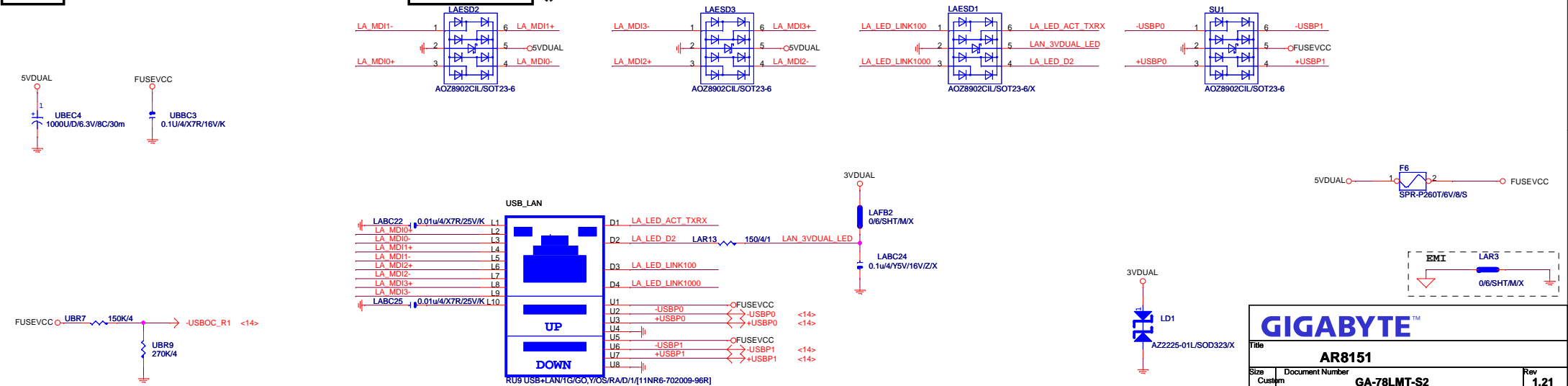


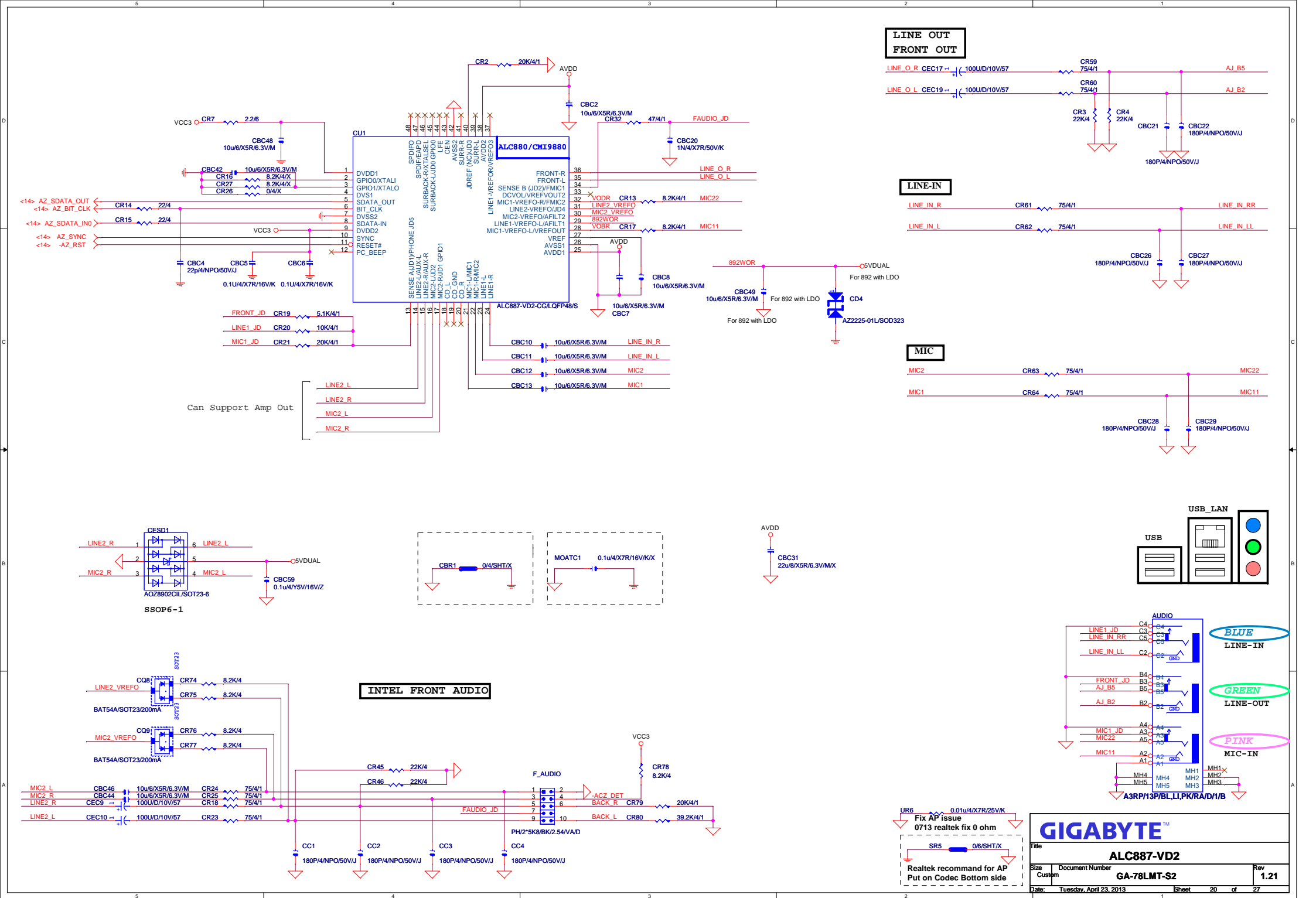
## Power domain chart

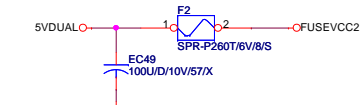
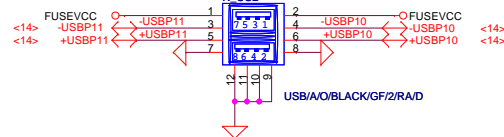
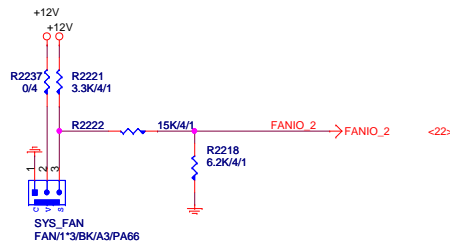
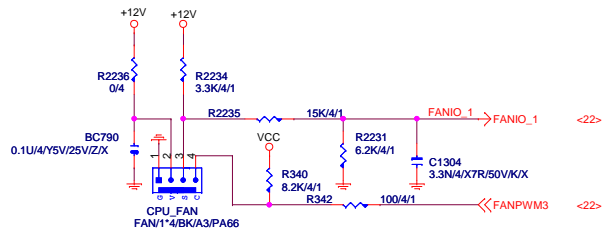
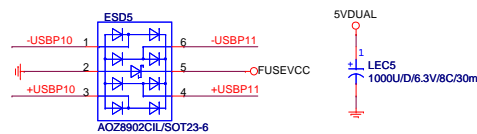
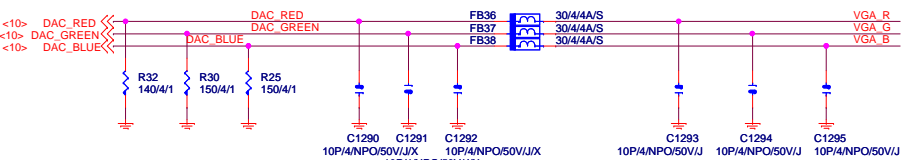
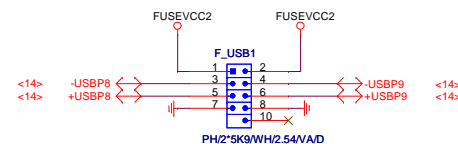
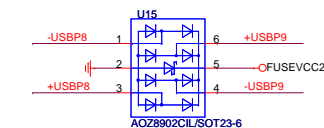
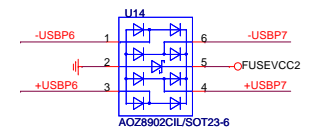
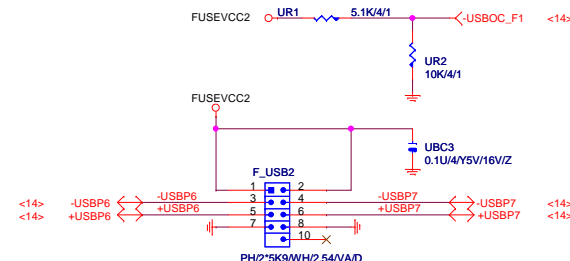
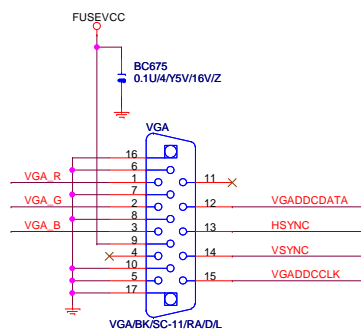
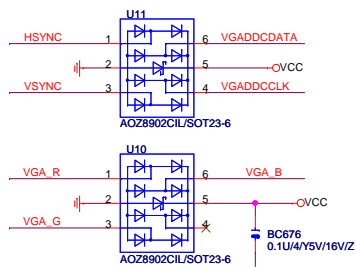
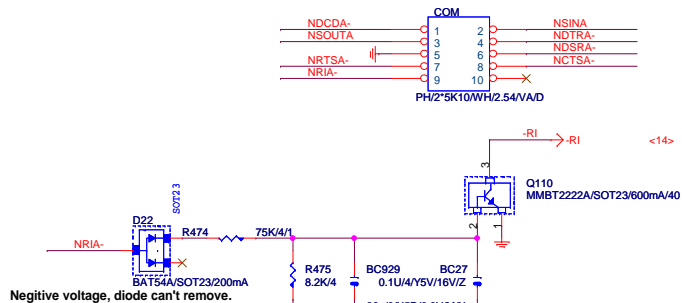
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

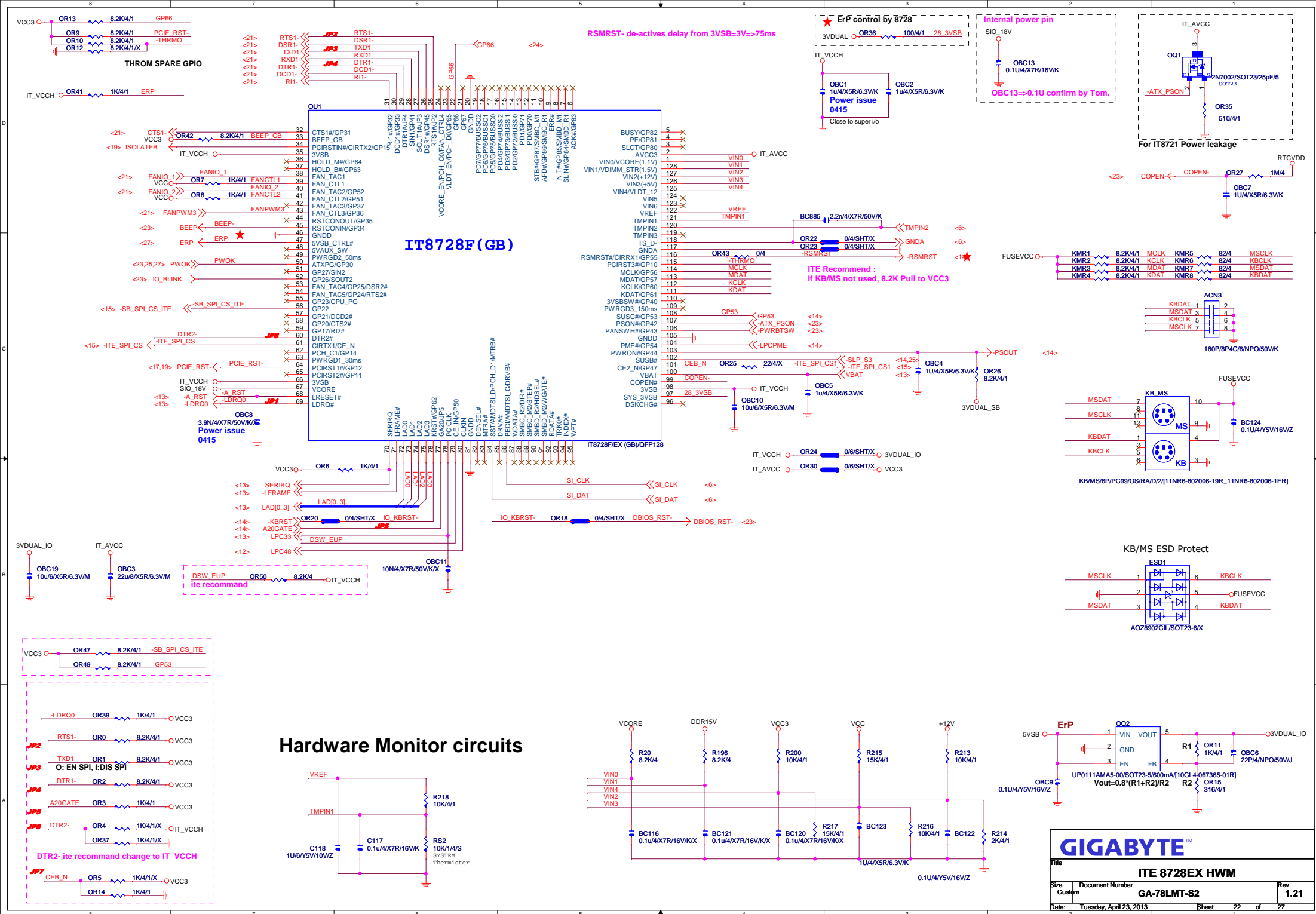


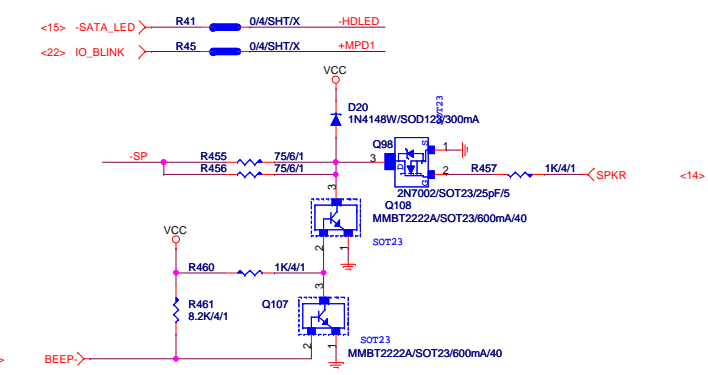
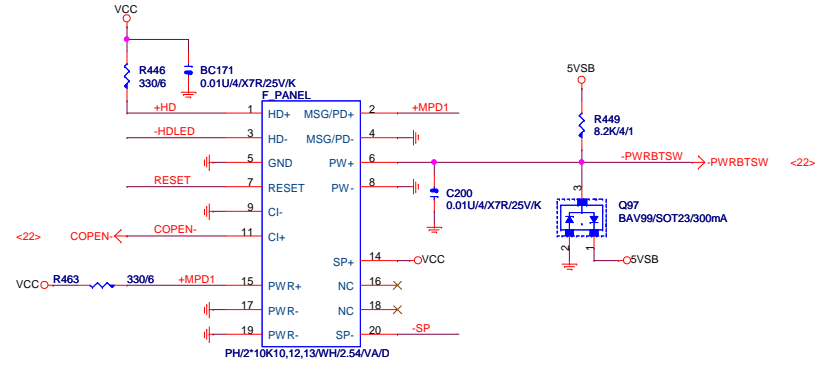
## MDI ESD預留28KV \*



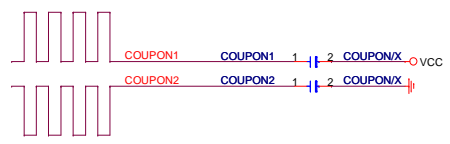
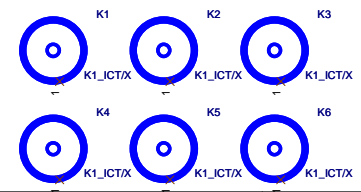
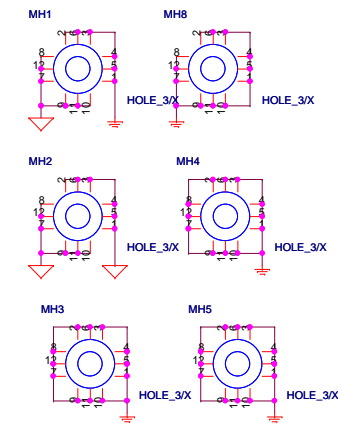
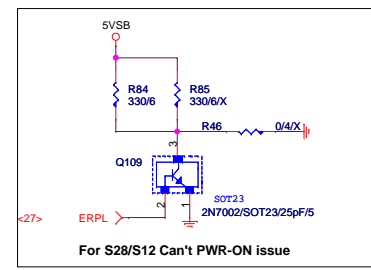
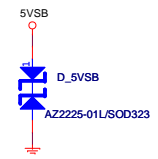
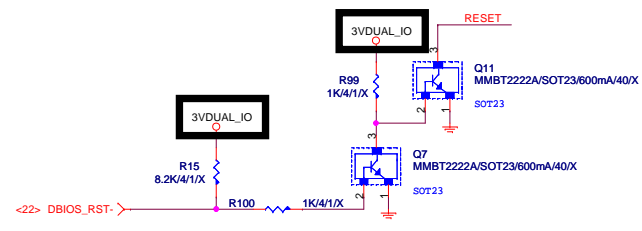
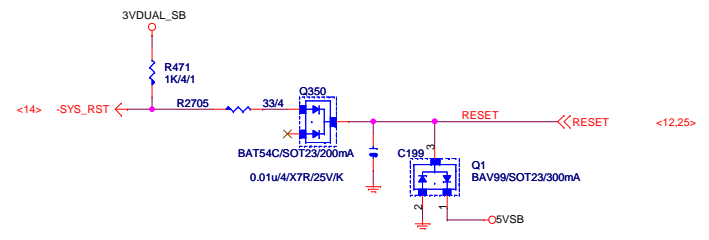
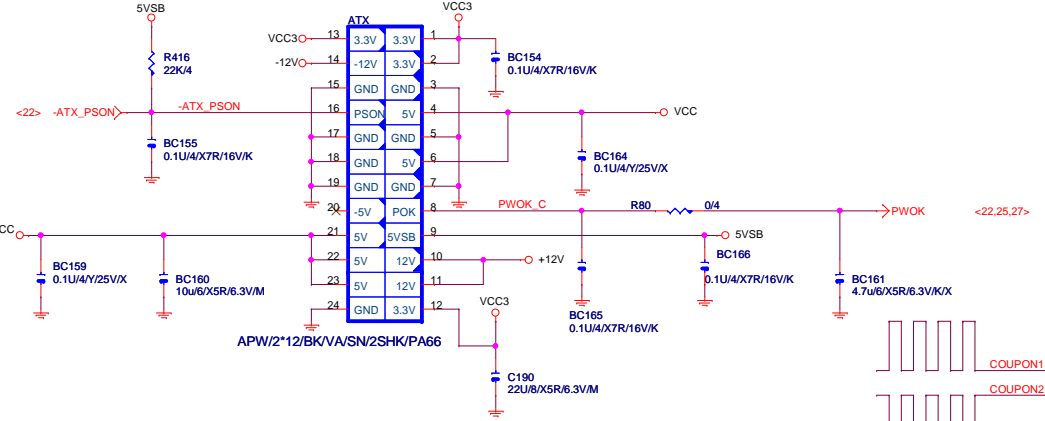


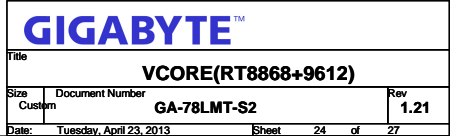






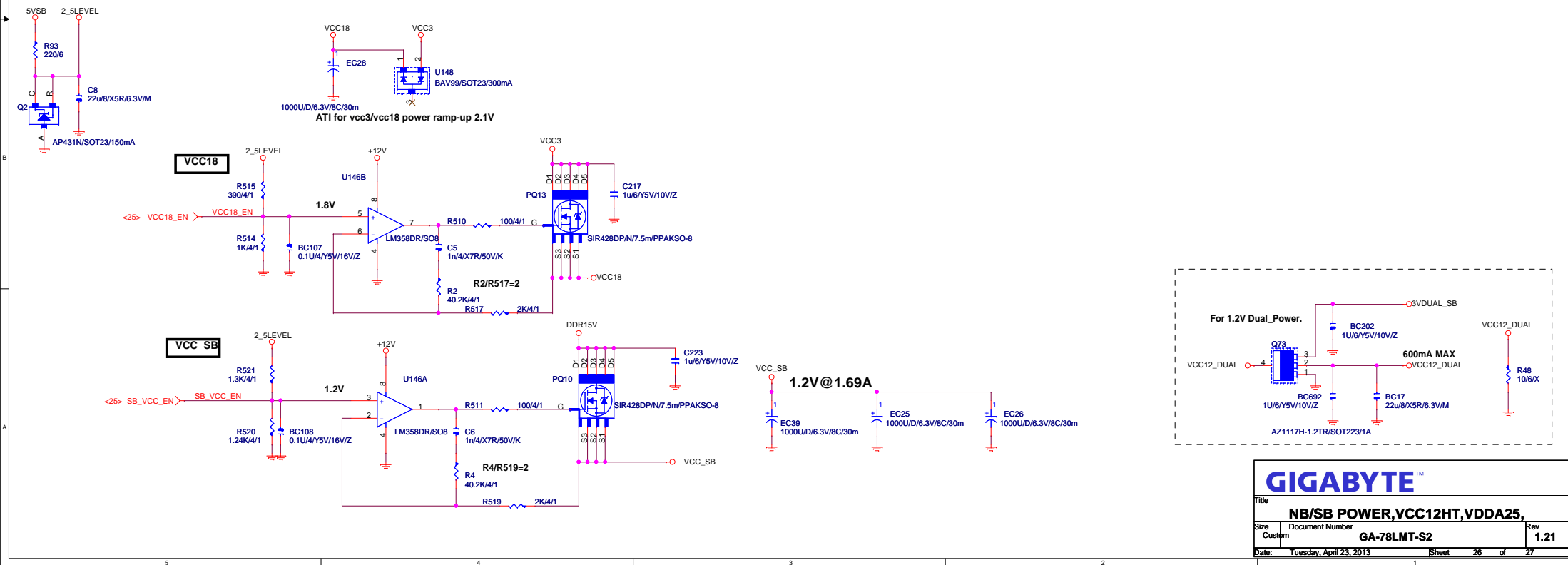
### ATX POWER CONNECTOR

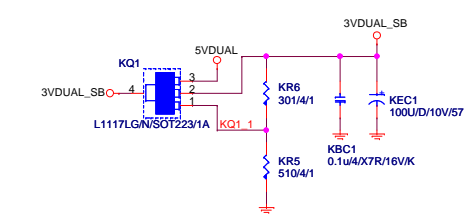
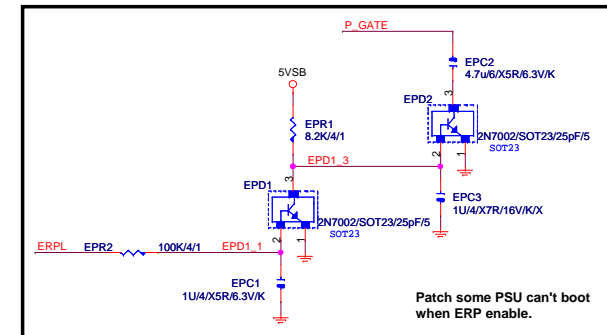
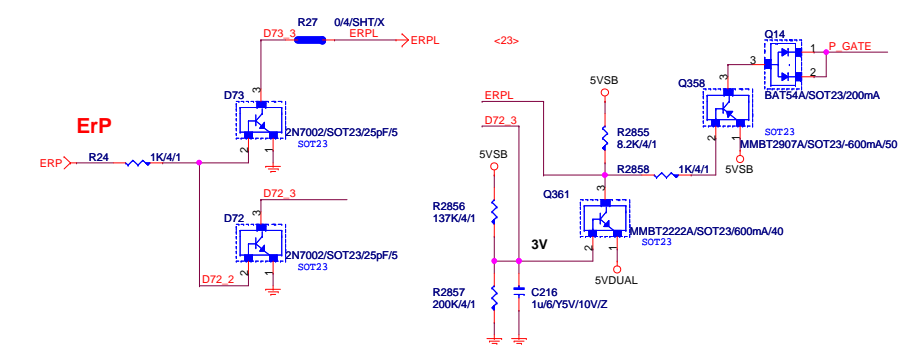
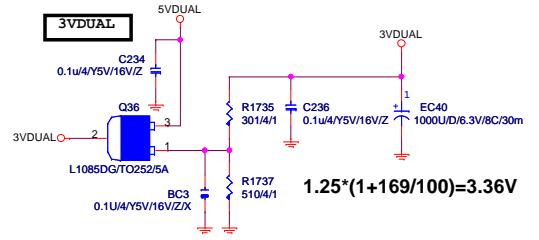
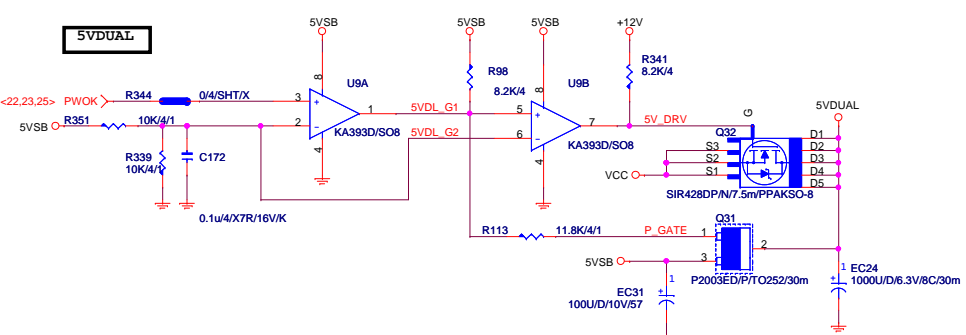




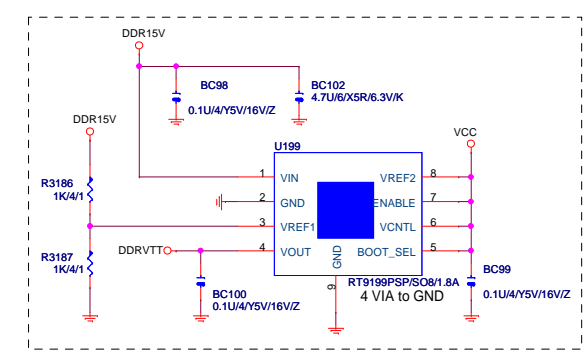
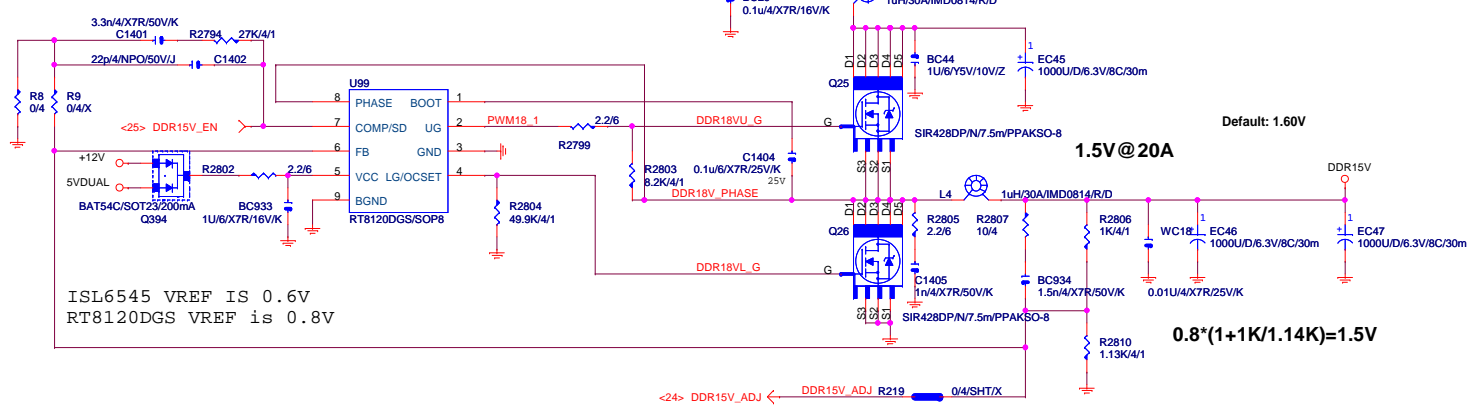








ISL6545 R9=>0, R8=>NC  
RT8120 R9=>NC, R8=>0



GIGABYTE™			
Title <b>DDR II POWER , VCC18</b>			
Size Custom	Document Number <b>GA-78LMT-S2</b>	Rev <b>1.21</b>	
Date: Tuesday, April 23, 2013	Sheet 27	of 27	